NATIONAL UNIVERSITY OF SCIENCES AND TECHNOLOGY
COLLEGE OF ELECTRICAL AND MECHANICAL ENGINEERING

DIGITAL SYSTEM DESIGN
LAB 1
DE30 (CE)

Submission: 19th Sep 2011

VERILOG CODING

Objective: The objective of the lab is to make students understand the working of the basic VERILOG syntax and their use. And also to understand how different blocks can be coded in VERILOG and how a stimulus (test bench) can help in testing the design for functional correctness.

Design Problems:

1. Write RTL VERILOG code to implement the design given in Figure 1. Generate appropriate reset signal for the feedback register used in the design. Write a stimulus to test the design for functional correctness (in stimulus use for-loop statement to provide different input values to your design).

   Optional: In stimulus count the number of cycles it takes for the register out reg to overflow for *in1* = 1 and *in2* = 1 and *sel* = 1, after the register is reset to 0.

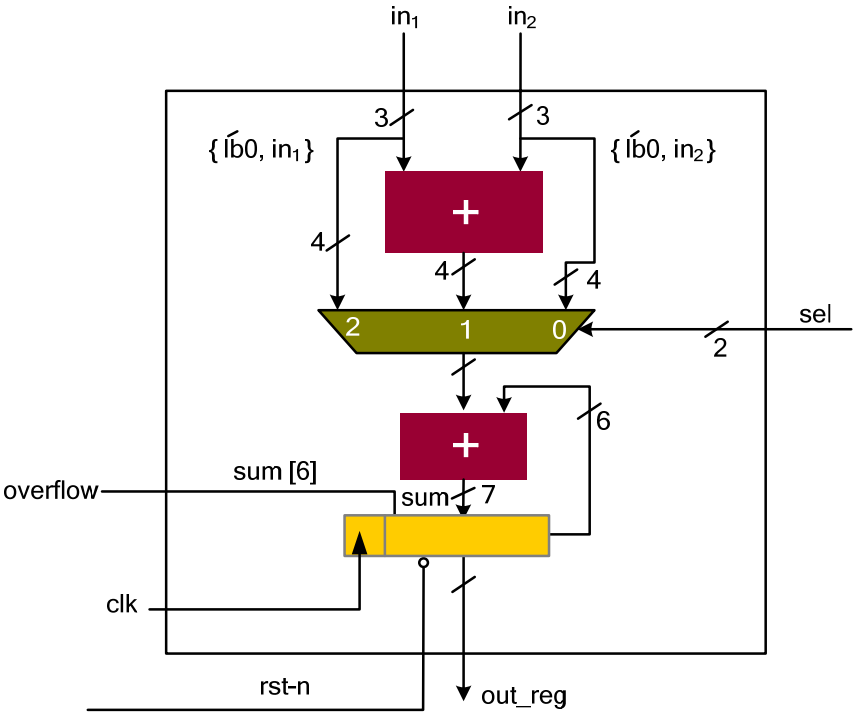

Figure 1: A digital design to be coded in RTL Verilog

2. Design an ALU datapath that performs the following operations in parallel on two 16 bit signed inputs A and B and assigns the value of one of the outputs to 16 bit C. The selection of operation is based on a 2 bit selection line. Code the design in VERILOG. Write test vectors to verify the implementation.
   C=A+B
   C=A-B
   C=A&B
   C=A|B